The example of recommendation of pattern is shown below Figure 22.
Pattern design is one of the critical items to determine power supply characteristics. In particular, that decides the stability of operation, EMI, the tolerance of surge. depends on pattern design. Moreover, having additional components to reduce noise might not be effective if pattern design has problems.

The countermeasure to reduce noise (e.g. additional components) can be most effective in case of ideal pattern design. Optimization of pattern design should be done as much as possible.

**PCB pattern design**

The example of recommendation of pattern is shown below Figure 22.
Pattern design is one of the critical items to determine power supply characteristics. In particular, that decides the stability of operation, EMI, the tolerance of surge. depends on pattern design. Moreover, having additional components to reduce noise might not be effective if pattern design has problems.

The countermeasure to reduce noise (e.g. additional components) can be most effective in case of ideal pattern design. Optimization of pattern design should be done as much as possible.

- **Legend**
  - ●: Improvement on noise
  - ▲: Stability enhancement on output line
  - ■: Stability enhancement on control
  - ◆: Enhancement on easier pattern design
  - ★: Enhancement on surge
  - ▼: Enhancement on heat dissipation

- **Pattern Colors**
  - Light yellow: Large fluctuation of voltage or high current line
  - Light blue: Stable voltage line
  - Blue: Most stable voltage line

- **Line Colors**
  - Red (solid line): Primary-side power loop
  - Red (dashed dotted line): Bias winding rectification loop
  - Red (dashed-two dotted line): Secondary-side rectification loop

- **TOP VIEW is shown this figure**

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Example of Recommended Pattern

(1) Power loop and the preceding line of input smoothing capacitor should be separated. (●●★▼)

(2) The preceding AC line of input filter and power loop should not be close. (●)

(3) Power loop should be short and thick. (●)

(4) Y capacitor should be located between input AC line and Drain. (★)

(5) All the patterns connected to Y capacitor should be short and thick as much as possible. (●★)

(6) Drain clamp circuit should be close to transformer. (●)

(7) GND pattern of power loop and IC control circuit should be separated. (■)

(8) The preceding AC line of input filter and power loop should not be close. (●)

(9) IS & VDD patterns should not be close to the pattern with large fluctuation of voltage (light yellow pattern in this figure) if possible. Stable potential pattern (light blue pattern in this figure) should be placed between the patterns with large fluctuation of voltage. RIS for noise filter should be placed close to IS pin. (■)

(10) Power loop and bias winding rectification loop should not be close to the control circuit pin and the connected patterns. (■)

(11) GND pattern of bias winding rectification loop and IC control circuit should be separated. (●■)

(12) Bias winding rectification loop should be short and thick as much as possible. (●)

(13) Electrolytic capacitor CVDD2 connected to VDD pin should be close to IC as much as possible. (●)

(14) Secondary-side rectification loop should be short and thick as much as possible. (●)

(15) Secondary-side rectification loop and the latter line of output capacitor should be separated. (●▲◆▼)

(16) The noise generated by Relays or lamps in AC line should not affect IC operation. (■, ★)

(17) Capacitor to remove noise should be placed close to each pin. (■★)

(18) IS & VDD patterns should not be close to the pattern with large fluctuation of voltage (light yellow pattern in this figure) if possible. Stable potential pattern (light blue pattern in this figure) should be placed between the patterns with large fluctuation of voltage. RIS for noise filter should be placed close to IS pin. (■)

- **Example of Recommended Pattern**

- **Pattern design is one of the critical items to determine power supply characteristics. In particular, that decides the stability of operation, EMI, the tolerance of surge. depends on pattern design. Moreover, having additional components to reduce noise might not be effective if pattern design has problems.**

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# Points to note and explanation on pattern design

<table>
<thead>
<tr>
<th>No.</th>
<th>Notes</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power loop &amp; Preceding line of input capacitor should be separated.</td>
<td>The pattern before/after rectification &amp; smoothing should be separated to prevent the noise generated in power loop from conducting into the preceding circuit of input capacitor. The pattern of connection point of input capacitor +/- pins should be narrow to flow all the current of power loop into input capacitor &amp; to make it difficult to conduct the heat generated by MOSFET to capacitor. In case of surge added in AC line, surge current conducts into input capacitor. Thus it is possible to prevent surge current from conducting into MOSFET directly.</td>
</tr>
<tr>
<td>2</td>
<td>Power loop &amp; the preceding AC line of input filter should not be near.</td>
<td>This design can prevent the noise generated inside power loop from conducting directly to the preceding AC line of input filter. The purpose of this is that the effectiveness of X capacitor and line filter can be maximized.</td>
</tr>
<tr>
<td>3</td>
<td>Power loop should be short &amp; thick as much as possible</td>
<td>Power loop flows high current with high frequency, and this current is the source of noise. Thus this loop should be short as much as possible and the area inside this loop should be small.</td>
</tr>
<tr>
<td>4</td>
<td>Y capacitor should be positioned between input AC line and Drain.</td>
<td>Y capacitor should be placed so that external noise such as surge from input line can not reach the drain of MOSFET and also Y capacitor can absorb it. It is important that the surge conducts to the connection point of Y capacitor.</td>
</tr>
<tr>
<td>5</td>
<td>The pattern connected to Y capacitor should be short &amp; thick as much as possible</td>
<td>The pattern towards Y capacitor could conduct the noise at primary-side to secondary-side, so this pattern should be short and thick as much as possible. Thus the impedance to Y capacitor can be decreased and noise reduction becomes effective.</td>
</tr>
<tr>
<td>6</td>
<td>Drain clamp circuit should be close to transformer as much as possible</td>
<td>The pattern from the components of drain clamp circuit to transformer or MOSFET should be short as much as possible. This pattern flows high current with high frequency which is the source of noise.</td>
</tr>
<tr>
<td>7</td>
<td>GND patterns of power loop &amp; IC control circuit should be separated.</td>
<td>GND of power loop is unstable, and GND pattern of power loop &amp; GND pattern of IC control circuit should be different circuit. Each input capacitor CIN should be connected at one point of CIN. The components related to IC control circuit should not be connected to power loop, and also GND pattern of control circuit should be as large as possible.</td>
</tr>
<tr>
<td>8</td>
<td>Capacitor to remove noise should be placed close to each pin.</td>
<td>Noise removal capacitors (IS/VDD/VC pin — GND pin ceramic capacitor) should not be connected to power loop. Moreover they should be near to each pin and GND pin as much as possible.</td>
</tr>
<tr>
<td>9</td>
<td>IS &amp; VDD patterns should not be close to patterns with large fluctuation of voltage (Bias winding rectification loop, TR pin pattern, Gate-OUT pattern, etc) if possible. Stable potential pattern (Primary-side stable GND, VCC, etc) should be positioned between patterns with large fluctuation of voltage.</td>
<td>A VDD terminal and IS terminal should be terminals which control a current peak value, and in a noise, since the feeding back line connected with these terminals is sensitive to a noise, TR terminal with an always large potential change and the OUT terminal should detach and arrange it. In order to prevent the noise from these patterns, the GND line (power loop GND removes) and VCC line (after bias winding rectification smooth) by the side of primary between feeding back lines. Moreover the resistor should be placed close to IS pin, and the pattern to connect IS pin with this resistor should be as short as possible.</td>
</tr>
<tr>
<td>10</td>
<td>Power loop and Bias winding rectification loop should not be close to the control circuit pins and the connected patterns.</td>
<td>Power loop and bias winding rectification loop generate large fluctuation of voltage or current with high frequency, and are the source of noise. Control circuit pins should keep enough distance to avoid any influence of this noise.</td>
</tr>
<tr>
<td>11</td>
<td>GND patterns of Rectification loop of bias winding &amp; IC control circuit should be separated.</td>
<td>GND of bias winding rectification loop is unstable, and GND pattern related to IC control circuit should be another circuit. Moreover all the components related to IC control circuit should not be connected to bias winding rectification loop.</td>
</tr>
<tr>
<td>12</td>
<td>Rectified loop of bias winding should be short &amp; thick as much as possible</td>
<td>Rectification diode of Bias winding should have short and thick pattern at anode side. The loop (Bias winding, Rectification diode, Smoothing capacitor) should be as short as possible, and no other components should be connected to this line.</td>
</tr>
<tr>
<td>13</td>
<td>Electrolytic capacitor CVDD2 connected to VDD pin should be located at the close position to IC as much as possible.</td>
<td>This product controls the feedback signal by VDD pin voltage. Thus CVDD2 and VDD pin should be placed nearby.</td>
</tr>
<tr>
<td>14</td>
<td>Secondary-side rectified loop should be short &amp; thick as much as possible</td>
<td>This is the loop with high current and high frequency like power loop. This loop should be as short as possible and the area inside this loop should be small.</td>
</tr>
<tr>
<td>15</td>
<td>Secondary-side rectification loop and the preceding line of output capacitor should be separated.</td>
<td>The pattern before/after rectification &amp; smoothing should be separated to prevent the noise generated in secondary-side rectification circuit from conducting into the latter circuit of output capacitor. Secondary-side rectification loop generates large fluctuation of voltage &amp; current with high frequency. The circuit of feedback &amp; output voltage detection should be connected to the pattern after rectification &amp; smoothing. Moreover The pattern of connection point of output smoothing capacitor +/- pins should be narrow to flow all the current in secondary-side loop into output smoothing capacitor &amp; to make it difficult to conduct the heat generated by output diode to capacitor.</td>
</tr>
<tr>
<td>16</td>
<td>The noise generated by Relays or lamps in AC line should not affect IC operation.</td>
<td>Any noise from the relays or lamps in AC line should not reach IC. ① IC should not be close to the source of noise or conducting path. ② Capacitor should be added to the source of noise. ③ Y capacitor etc should be located in the conducting path of noise.</td>
</tr>
</tbody>
</table>
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